3.3V Dual LVTTL/LVCMOS to Differential LVPECL Translator

Description

The MC100LVELT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

Features

- 350 ps Typical Propagation Delay
- <100 ps Output-to-Output Skew
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range: V_{CC} = 3.0 V to 3.8 V with GND = 0 V
- When Unused TTL Input is left Open, Q Output will Default High
- Pb-Free Packages are Available



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MARKING DIAGRAMS*



SOIC-8 D SUFFIX CASE 751





TSSOP-8 DT SUFFIX CASE 948R





DFN8 MN SUFFIX CASE 506AA



A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

 \overline{M} = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

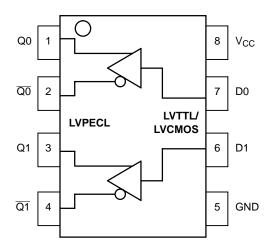


Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|--|---|
| Qn, Qn D0, D1 V _{CC} GND | LVPECL Differential Outputs LVTTL/LVCMOS Inputs Positive Supply Ground |
| EP | Exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply or leave floating open. |

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

ΕP

Table 2. ATTRIBUTES

| Charac | Value | | | | |
|--|-----------------------------------|----------------------|--|--|--|
| Internal Input Pulldown Resisto | N/A | | | | |
| Internal Input Pullup Resistor | N/A | | | | |
| ESD Protection | Human Body Model Machine Model | > 4 kV > 200 V | | | |
| Moisture Sensitivity, Indefinite | Fime Out of Drypack (Note 1) | Level 1 | | | |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | | | |
| Transistor Count | | 164 | | | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | | | |

^{1.} For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|-------------------|--|--|---------------------|---------------|--------------|
| V _{CC} | Positive Power Supply | GND = 0 V | | 7 | V |
| VI | Input Voltage | GND = 0 V | $V_{I} \leq V_{CC}$ | 7 | V |
| l _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SO-8 SO-8 | 190 130 | °C/W |
| θЈС | Thermal Resistance (Junction-to-Case) | std bd | SO-8 | 41 to 44 ± 5% | °C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | TSSOP-8 TSSOP-8 | 185 140 | °C/W |
| $\theta_{\sf JC}$ | Thermal Resistance (Junction-to-Case) | std bd | TSSOP-8 | 41 to 44 ± 5% | °C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | DFN8 DFN8 | 129 84 | °C/W °C/W |
| T _{sol} | Wave Solder Pb Pb-Free | <2 to 3 sec @ 248°C <2 to 3 sec @ 260°C | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0.0 V (Note 2)

| | | -40°C | | 25°C | | 85°C | | | | | |
|-----------------|------------------------------|-------|-----|------|------|------|------|------|-----|------|------|
| Symbol | Characteristic | Min | Тур | Max | Min | Тур | Max | Min | Тур | Max | Unit |
| I _{CC} | Power Supply Current | | | 28 | | | 28 | | | 29 | mA |
| V _{OH} | Output HIGH Voltage (Note 3) | 2275 | | 2420 | 2275 | | 2420 | 2275 | | 2420 | mV |
| V _{OL} | Output LOW Voltage (Note 3) | 1490 | | 1680 | 1490 | | 1680 | 1490 | | 1680 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 2. Output parameters vary 1:1 with V_{CC} . V_{CC} can vary ± 0.15 V. 3. Outputs are terminated through a 50 ohm resistor to V_{CC} –2 volts.

Table 5. LVTTL/LVCMOS INPUT DC CHARACTERISTICS $V_{CC} = 3.3 \text{ V}$; $T_A = -40 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$ (Note 4)

| Symbol | Characteristic | Min | Тур | Max | Unit | Condition |
|------------------|--------------------|-----|-----|------|------|---------------------------|
| I _{IH} | Input HIGH Current | | | 20 | μΑ | V _{IN} = 2.7 V |
| I _{IHH} | Input HIGH Current | | | 100 | μΑ | $V_{IN} = V_{CC}$ |
| I₁∟ | Input LOW Current | | | -0.2 | mA | V _{IN} = 0.5 V |
| V _{IK} | | | | -1.2 | V | $I_{IN} = -18 \text{ mA}$ |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. V_{CC} can vary ± 0.15 V.

Table 6. AC CHARACTERISTICS $V_{CC} = 3.3 \text{ V}$; GND = 0.0 V (Note 5)

| | | | -40°C | | 25°C | | 85°C | | | | | |
|------------------|---------------------------|----------------------------------|-------|-----|------------|-----|------|------------|-----|-----|------------|------|
| Symbol | С | haracteristic | Min | Тур | Max | Min | Тур | Max | Min | Тур | Max | Unit |
| f _{max} | Maximum Toggle Frequency | | | | | | 350 | | | | | MHz |
| t _{PLH} | Propagation D | Delay (Note 6) | 200 | 350 | 600 | 200 | 350 | 600 | 200 | 350 | 600 | ps |
| t skew | Skew | Output-to-Output Part-to-Part | | 30 | 100 400 | | 30 | 100 400 | | 30 | 100 400 | ps |
| tJITTER | Random Clock Jitter (RMS) | | | | | | 1.6 | | | | | ps |
| t /t r f | Output Rise/F | all Time (20-80%) | 200 | | 550 | 200 | | 500 | 200 | | 500 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 5. V_{CC} can vary ± 0.15 V.
- 6. Specifications for standard TTL input signal.

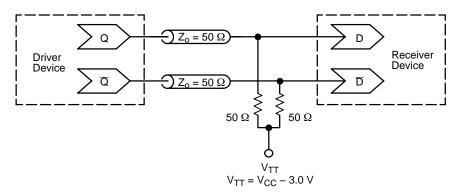


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-------------------|----------------------|-----------------------|
| MC100LVELT22D | SOIC-8 | 98 Units / Rail |
| MC100LVELT22DG | SOIC-8 (Pb-Free) | 98 Units / Rail |
| MC100LVELT22DR2 | SOIC-8 | 2500 / Tape & Reel |
| MC100LVELT22DR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LVELT22DT | TSSOP-8 | 100 Units / Rail |
| MC100LVELT22DTG | TSSOP-8 (Pb-Free) | 100 Units / Rail |
| MC100LVELT22DTR2 | TSSOP-8 | 2500 / Tape & Reel |
| MC100LVELT22DTR2G | TSSOP-8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LVELT22MNR4 | DFN8 | 1000 / Tape & Reel |
| MC00LVELT22MNR4G | DFN8 (Pb-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D - ECL Clock Distribution Techniques
AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS ™ I/O SPICE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL
AN1672/D – The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

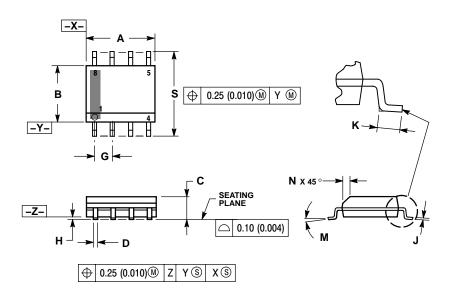
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

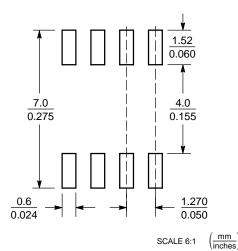
SOIC-8 NB CASE 751-07 **ISSUE AH**



- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- AND 114-3M, 1962.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A AND B DO NOT INCLUDE
 MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| | MILLIN | IETERS | INC | HES | |
|-----|--------|---------|-----------|-------|--|
| DIM | MIN | MIN MAX | | MAX | |
| Α | 4.80 | 5.00 | 0.189 | 0.197 | |
| В | 3.80 | 4.00 | 0.150 | 0.157 | |
| С | 1.35 | 1.75 | 0.053 | 0.069 | |
| D | 0.33 | 0.51 | 0.013 | 0.020 | |
| G | 1.27 | 7 BSC | 0.050 BSC | | |
| Н | 0.10 | 0.25 | 0.004 | 0.010 | |
| J | 0.19 | 0.25 | 0.007 | 0.010 | |
| K | 0.40 | 1.27 | 0.016 | 0.050 | |
| M | 0 ° | 8 ° | 0 ° | 8 ° | |
| Ν | 0.25 | 0.50 | 0.010 | 0.020 | |
| 5 | 5.80 | 6.20 | 0.228 | 0 244 | |

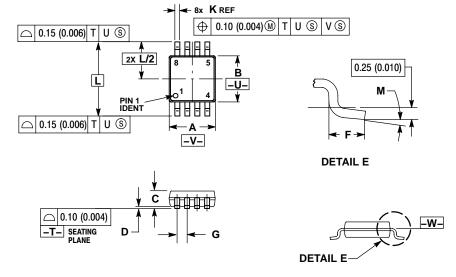
SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-8 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948R-02 **ISSUE A**



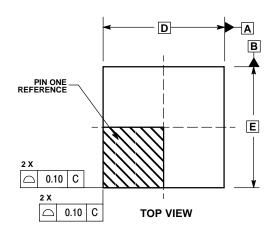
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

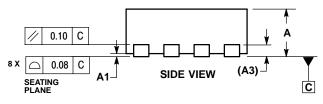
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

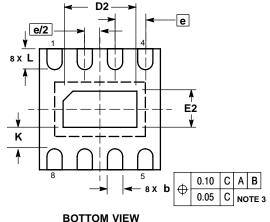
| | MILLIN | IETERS | INC | HES |
|-----|--------|--------|-------|-------|
| DIM | MIN | MAX | MIN | MAX |
| Α | 2.90 | 3.10 | 0.114 | 0.122 |
| В | 2.90 | 3.10 | 0.114 | 0.122 |
| С | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 | BSC | 0.026 | BSC |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 | BSC | 0.193 | BSC |
| М | 0° | 6° | 0° | 6° |

PACKAGE DIMENSIONS

DFN8 CASE 506AA-01 ISSUE D







- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994 TO LERANGING FER ASME Y14.5M, 1994 CONTROLLING DIMENSION: MILLIMETERS. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | | | | | |
|-----|-------------|----------|--|--|--|--|
| DIM | MIN MAX | | | | | |
| Α | 0.80 | 1.00 | | | | |
| A1 | 0.00 | 0.05 | | | | |
| A3 | 0.20 | REF | | | | |
| b | 0.20 | 0.30 | | | | |
| D | 2.00 | BSC | | | | |
| D2 | 1.10 | 1.30 | | | | |
| E | 2.00 | BSC | | | | |
| E2 | 0.70 | 0.90 | | | | |
| е | 0.50 | 0.50 BSC | | | | |
| K | 0.20 | | | | | |
| L | 0.25 | 0.35 | | | | |

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